MCP6271/1R/2/3/4/5

170 µA, 2 MHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 2 MHz (typical)
- Supply Current: I_Q = 170 µA (typical)
- Supply Voltage: 2.0V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range: –40°C to +125°C
- Available in Single, Dual and Quad Packages
- Parts with Chip Select ($\overline{CS}$)
  - Single (**MCP6273**)
  - Dual (**MCP6275**)

Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery Powered Systems

Available Tools

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Description

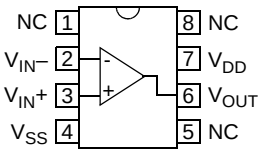
The Microchip Technology Inc. MCP6271/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 2 MHz Gain Bandwidth Product (GBWP) and a 65° Phase Margin. This family also operates from a single supply voltage as low as 2.0V, while drawing 170 µA (typical) quiescent current. The MCP6271/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6275 has a Chip Select input ($\overline{CS}$) for dual op amps in an 8-pin package and is manufactured by cascading two op amps (the output of op amp A connected to the non-inverting input of op amp B). The $\overline{CS}$ input puts the device in low power mode.

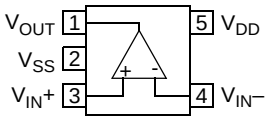
The MCP6271/1R/2/3/4/5 family operates over the Extended Temperature Range of –40°C to +125°C, with a power supply range of 2.0V to 6.0V.

Package Types

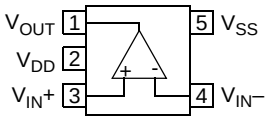
MCP6271
PDIP, SOIC, MSOP



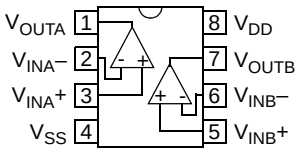
MCP6271
SOT-23-5



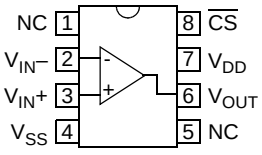
MCP6271R
SOT-23-5



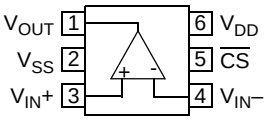
MCP6272
PDIP, SOIC, MSOP



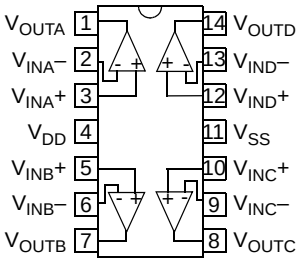
MCP6273
PDIP, SOIC, MSOP



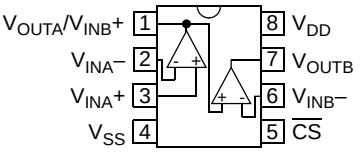
MCP6273
SOT-23-6



MCP6274
PDIP, SOIC, TSSOP



MCP6275
PDIP, SOIC, MSOP



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† .. V_{SS} – 1.0V to V_{DD} + 1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....–65°C to +150°C
Junction Temperature (T_J) .....+150°C
ESD Protection On All Pins (HBM/MM) ..... ≥ 4 kV/400V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset (Note 1)						
Input Offset Voltage	V_{OS}	–3.0	—	+3.0	mV	$V_{CM} = V_{SS}$
Input Offset Voltage (Extended Temperature)	V_{OS}	–5.0	—	+5.0	mV	T_A = –40°C to +125°C, $V_{CM} = V_{SS}$
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±1.7	—	µV/°C	T_A = –40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	70	90	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1.0	—	pA	**Note 2**
At Temperature	I_B	—	50	200	pA	T_A= +85°C **(Note 2)**
At Temperature	I_B	—	2	5	nA	T_A= +125°C **(Note 2)**
Input Offset Current	I_{OS}	—	±1.0	—	pA	**Note 3**
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	**Note 3**
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	**Note 3**
Common Mode (Note 4)						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.15	—	V_{DD} + 0.15	V	V_{DD} = 2.0V **(Note 5)**
	V_{CMR}	V_{SS} – 0.30	—	V_{DD} + 0.30	V	V_{DD} = 5.5V **(Note 5)**
Common Mode Rejection Ratio	CMRR	70	85	—	dB	V_{CM} = –0.3V to 2.5V, V_{DD} = 5V **(Note 6)**
Common Mode Rejection Ratio	CMRR	65	80	—	dB	V_{CM} = –0.3V to 5.3V, V_{DD} = 5V **(Note 6)**
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB	V_{OUT} = 0.2V to V_{DD} – 0.2V, $V_{CM} = V_{SS}$ **(Note 1)**

Note 1: The MCP6275's V_{CM} for op amp B (pins V_{OUTA}/V_{INB}+ and V_{INB}–) is V_{SS} + 100 mV.
2: The current at the MCP6275's V_{INB}– pin is specified by I_B only.
3: This specification does not apply to the MCP6275's V_{OUTA}/V_{INB}+ pin.
4: The MCP6275's V_{INB}– pin (op amp B) has a common mode input voltage range (V_{CMR}) of V_{SS} + 100 mV to V_{DD} – 100 mV. CMRR is not measured for op amp B of the MCP6275. The MCP6275's V_{OUTA}/V_{INB}+ pin (op amp B) has a voltage range specified by V_{OH} and V_{OL}.
5: Set by design and characterization.
6: Does not apply to op amp B of the MCP6275.
7: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 2.0V and 5.5V.

DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 15	mV	0.5V input overdrive **(Note 4)**
Output Short Circuit Current	I_{SC}	—	±25	—	mA	
Power Supply						
Supply Voltage	V_{DD}	2.0	—	6.0	V	
Quiescent Current per Amplifier	I_Q	100	170	240	µA	I_O = 0

Note 1: The MCP6275's V_{CM} for op amp B (pins V_{OUTA}/V_{INB}+ and V_{INB}–) is V_{SS} + 100 mV.

2: The current at the MCP6275's V_{INB}– pin is specified by I_B only.

3: This specification does not apply to the MCP6275's V_{OUTA}/V_{INB}+ pin.

4: The MCP6275's V_{INB}– pin (op amp B) has a common mode input voltage range (V_{CMR}) of V_{SS} + 100 mV to V_{DD} – 100 mV. CMRR is not measured for op amp B of the MCP6275. The MCP6275's V_{OUTA}/V_{INB}+ pin (op amp B) has a voltage range specified by V_{OH} and V_{OL}.

5: Set by design and characterization.

6: Does not apply to op amp B of the MCP6275.

7: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 2.0V and 5.5V.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	0.9	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	4.6	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	20	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

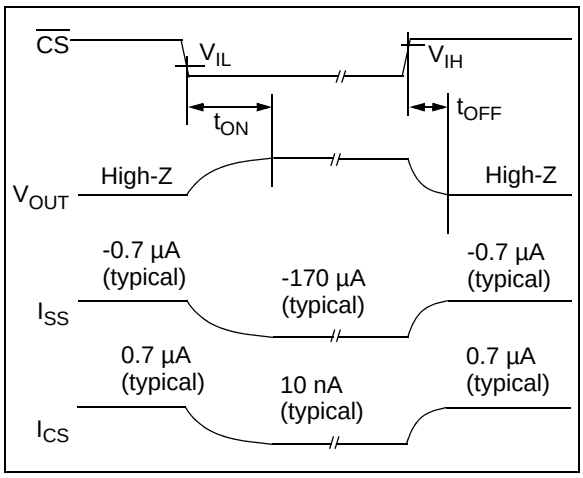


FIGURE 1-1: *Timing Diagram for the Chip Select ($\overline{CS}$) pin on the MCP6273 and MCP6275.*

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.0V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	–40	—	+125	°C	
Operating Temperature Range	T_A	–40	—	+125	°C	**Note**
Storage Temperature Range	T_A	–65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

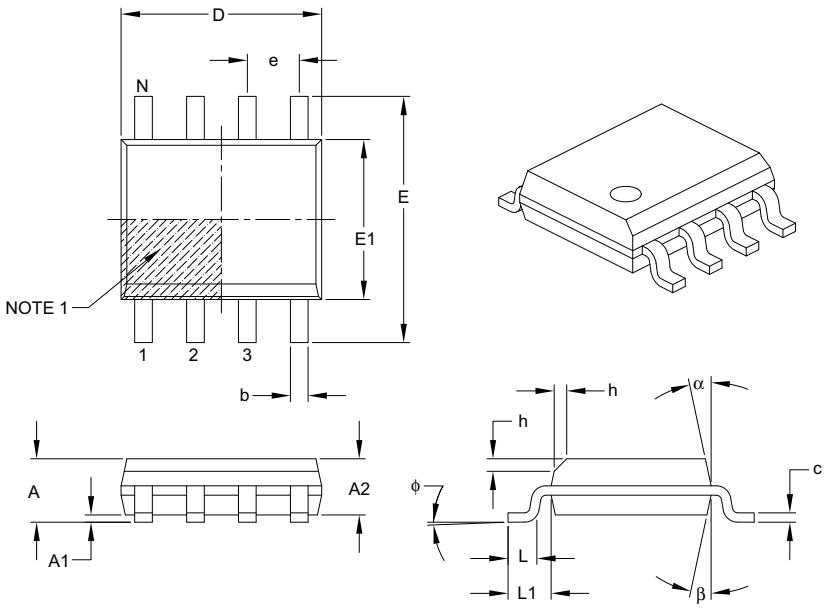
Note: The Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

MCP6273/MCP6275 CHIP SELECT SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$, C_L = 60 pF and $\overline{CS}$ is tied low.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2V_{DD}$	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	0.01	—	µA	$\overline{CS} = V_{SS}$
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	$0.8V_{DD}$	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2	µA	$\overline{CS} = V_{DD}$
GND Current per Amplifier	I_{SS}	—	–0.7	—	µA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage	—	—	0.01	—	µA	$\overline{CS} = V_{DD}$
Dynamic Specifications (Note 1)						
$\overline{CS}$ Low to Valid Amplifier Output, Turn on Time	t_{ON}	—	4	10	µs	$\overline{CS}$ Low ≤ 0.2 V_{DD}, G = +1 V/V, $V_{IN} = V_{DD}/2$, V_{OUT} = 0.9 $V_{DD}/2$, V_{DD} = 5.0V
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	0.01	—	µs	$\overline{CS}$ High ≥ 0.8 V_{DD}, G = +1 V/V, $V_{IN} = V_{DD}/2$, V_{OUT} = 0.1 $V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5V

Note 1: The input condition (V_{IN}) specified applies to both op amp A and B of the MCP6275. The dynamic specification is tested at the output of op amp B (V_{OUTB}).

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX
Device		Temperature Range	Package

Device:	MCP6271:	Single Op Amp
	MCP6271T:	Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5)
	MCP6271RT:	Single Op Amp (Tape and Reel) (SOT-23-5)
	MCP6272:	Dual Op Amp
	MCP6272T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)
	MCP6273:	Single Op Amp with Chip Select
	MCP6273T:	Single Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP, SOT-23-6)
	MCP6274:	Quad Op Amp
	MCP6274T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)
	MCP6275:	Dual Op Amp with Chip Select
	MCP6275T:	Dual Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP)
Temperature Range:	E =	-40°C to +125°C
Package:	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6271, MCP6271R)
	CH =	Plastic Small Outline Transistor (SOT-23), 6-lead (MCP6273)
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC, (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP (4.4 mm Body), 14-lead

Examples:

a)	MCP6271-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6271-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6271-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6271T-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6271RT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6272-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6272-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6272-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6272T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package.
a)	MCP6273-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6273-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6273-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6273T-E/CH:	Extended Temperature, 6LD SOT-23 package.
a)	MCP6274-E/P:	Extended Temperature, 14LD PDIP package.
b)	MCP6274T-E/SL:	Tape and Reel, Extended Temperature, 14LD SOIC package.
c)	MCP6274-E/SL:	Extended Temperature, 14LD SOIC package.
d)	MCP6274-E/ST:	Extended Temperature, 14LD TSSOP package.
a)	MCP6275-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6275-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6275-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6275T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package.