TPS6123x High Efficiency Synchronous Step Up Converters with 5-A Switches

1 Features

- Input Voltage Range: 2.3 V to 5.5 V
- Output Voltage Range: 2.5 V to 5.5 V
- Up to 96% Efficiency Synchronous Boost Converter
- 3.3-V to 5-V Power Conversion with 2.1-A Output Current
- Input Supply Voltage Supervisor with Adjustable Threshold/Hysteresis
- Power Save Mode for Light Load Efficiency
- Load Disconnect During Shutdown
- Output Over Voltage Protection
- Programmable Soft Start
- Power Good Output
- 2-MHz Switching Frequency
- Output Capacitor Discharge (TPS61231)
- 3 mm x 3 mm x 0.9 mm VSON Package

2 Applications

- Low Voltage Li-Ion Battery Powered Products
- USB Power Supply
- Tablet PCs
- Power Banks, Battery Backup Units
- Industrial Metering Equipments

3 Description

The TPS6123x device family is a high efficiency synchronous step up converter with compact solution size. It is optimized for products powered by a one-cell Li-Ion battery, or a regulated power rail of 3.3 V. The IC integrates a 5-A switch and is capable of delivering output currents up to 2.1 A at a 5-V output with a 3.3-V input supply. The device is based on a quasi-constant on-time valley current mode control scheme. The typical operating frequency is 2 MHz, which allows the use of small inductors and capacitors to achieve a small solution size. The TPS61230 and TPS61231 provide an adjustable output voltage via an external resistor divider, and the TPS61232 provides a fixed output voltage of 5 V.

During light loads, the TPS6123x automatically enters power save mode for maximum efficiency at lowest quiescent currents. In shutdown, the load is completely disconnected from the input, and the input current consumption is reduced to 1.5 µA typical. The device integrates a precise low power EN comparator. The EN threshold as well as the hysteresis of the enable comparator are adjustable with external resistors and support application specific system power up and down requirements. Other features like output over voltage protection, thermal shutdown protection, and a power good output are built-in.

The devices are available in a 3 mm x 3 mm x 0.9 mm VSON package.

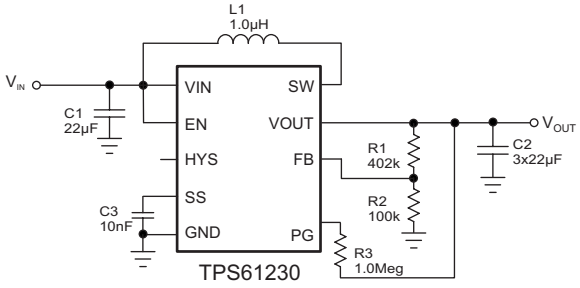
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61230	VSON (10)	3.00 mm x 3.00 mm
TPS61231(2)		
TPS61232		

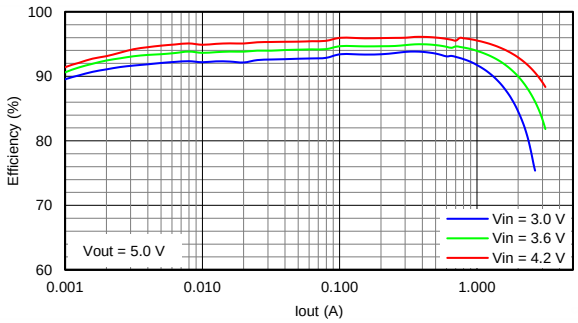
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Preview product. Contact TI factory for more information

TPS61230 Typical Application



TPS61230 Typical Application Efficiency



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4 Revision History

Changes from Revision B (June 2014) to Revision C — **Page**

- Changed Electrical Characteristics in the I_Q row; V_{OUT} = 3.5 V to V_{OUT} = No Supply ... 5

Changes from Revision A (March 2014) to Revision B — **Page**

- Added TPS61232 to the data sheet ... 1
- Changed the Device Information ... 1
- Changed the Device Comparison Table ... 3
- Changed the Handling Ratings table ... 4

Changes from Original (September 2013) to Revision A — **Page**

- Deleted TPS61232 from the data sheet ... 1
- Changed the data sheet to the new TI format ... 1
- Changed the Description From: input current consumption is reduced to 0.5 µA typical To: input current consumption is reduced to 1.5 µA typical ... 1
- Changed the Functional Block Diagram. Removed Note 2 ... 8
- Deleted the Programming The Output Voltage section ... 13
- Changed Figure 14 label From: Startup (A) To: Startup (Ω) ... 15

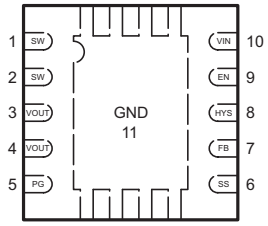
5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	OUTPUT DISCHARGE
TPS61230DRC	Adjustable	No
TPS61231DRC(1)	Adjustable	Yes
TPS61232DRC	5-V fixed output	No

(1) Preview product. Contact TI factory for more information

6 Pin Configuration and Functions

11-PIN VSON
DRC PACKAGE
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SW	1,2	PWR	The switch pin of the converter. It is connected to the drain of the internal Power MOSFETs.
VOUT	3,4	PWR	Boost converter output pin.
PG	5	OUT	Power Good open drain output. Can be left floating if not used.
SS	6	IN	Soft startup pin. A soft startup capacitor connects to this pin to set the soft start time.
FB	7	IN	Voltage feedback of adjustable versions. Must be connected to VOUT on fixed output voltage version.
HYS	8	OUT	EN hysteresis program pin. See the application section for details. Can be left floating if not used.
EN	9	IN	Enable logic input. Logic HIGH enables the device. Logic LOW disables the device and turns it into shutdown mode. This pin must be terminated.
VIN	10	IN	Supply voltage pin.
GND	11	PWR	Ground pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at pins(2)	EN, FB, PG, SS, HYS, VIN, VOUT, SW	–0.3	7	V
Operating junction temperature range, T_J		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground pin.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage at VIN pin	2.3		5.5	V
I_{SINK_PG}	Sink current at PG pin			500	µA
V_{PG}	Pull-up resistor voltage			5.5	V
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6123x	UNIT
		DRC (11 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	57.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	26.6	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	23.8	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	4.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 125°C and V_{IN} = 3.6 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{UVLO}	Input under voltage lockout	V_{IN} falling		2.0	2.1	V
		V_{IN} rising		2.1	2.2	
I_Q	Quiescent current into VIN	IC enabled, No load, No switching V_{OUT} = 5 V, T_J = –40 °C to 85°C		35	60	µA
		IC enabled, No load V_{IN} = 4.2 V, V_{OUT} = No supply, T_J = –40 °C to 85°C		200	230	
I_{SD}	Shutdown current into VIN	0 V ≤ V_{EN} ≤ 0.4 V, V_{IN} = 2.3 V to 5.5 V, T_J = -40 °C to 85°C		1.5	6	µA
	Leakage current from SW to VOUT	V_{EN} = 0 V, V_{OUT} = 0 V; V_{SW} = V_{IN} = 3.6 V			2.5	µA
OUTPUT						
V_{OUT}	Output voltage range		2.5		5.5	V
V_{OUT}	Output voltage accuracy, TPS61232	PWM mode	4.9	5.0	5.1	V
V_{OUT}	Output voltage accuracy, TPS61232	PFM mode(1)		5.035		V
V_{FB}	Feedback voltage, TPS61230 and TPS61231	PWM mode	0.985	1	1.015	V
		PFM mode(1)		1.007		
	FB pin leakage current	V_{FB} = 1 V			100	nA
R_{DIS}	Output discharge resistor TPS61231	V_{OUT} = 5 V		200		Ω
V_{OVP}	Over voltage protection DC threshold	V_{OUT} rising	5.7	6	6.2	V
	Over voltage protection hysteresis	V_{OUT} falling below V_{OVP}		0.15		
I_{SS}	Bias current in soft start phase	After pre-charge phase		5		µA
	Line regulation	I_{OUT} = 1 A, V_{IN} = 2.3 V to 4.5 V		0.06		%/V
	Load regulation	I_{OUT} = 0.5 A to 2 A		0.15		%/A
LOGIC INTERFACE						
$V_{TH\_EN\_ON}$	EN pin threshold rising	V_{IN} = 2.3 V to 5.5 V	1.15	1.19	1.23	V
$V_{TH\_EN\_OFF}$	EN pin threshold falling	V_{IN} = 2.3 V to 5.5 V	1.11	1.14	1.18	V
V_{OL_HYS}	HYS pin low level voltage	I_{SINK_HYS} = 1 mA, V_{EN} = 1.1 V			0.7	V
V_{TH_PG}	Power good DC threshold	V_{OUT} rising, referenced to $V_{OUT\_NOMINAL}$	93%	95%	99%	
		V_{OUT} falling referenced to $V_{OUT\_NOMINAL}$	87%	90%	93%	
V_{OL_PG}	PG pin low level voltage	I_{SINK_PG} = 500 µA			0.4	V
POWER STAGE						
I_{LIM_SW}	Switch valley current limit		4.0	5.0	6.0	A
I_{LIM_Pre}	Precharge current limit	V_{OUT} = 5 V	2.0	2.8	3.5	A
		V_{OUT} = 3.5 V	1.8	2.6	3.3	
		V_{OUT} = 0 V	0.4	0.55	0.7	
$R_{DS(on)}$	High side MOSFET on resistance	V_{OUT} = 5 V		50	75	mΩ
	Low side MOSFET on resistance	V_{OUT} = 5 V		50	75	
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling below T_{JSD}		20		

(1) L = 1 µH, C_{OUT} = 20 µF (effective capacitance value)

7.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = -40°C to 125 °C, unless otherwise noted.

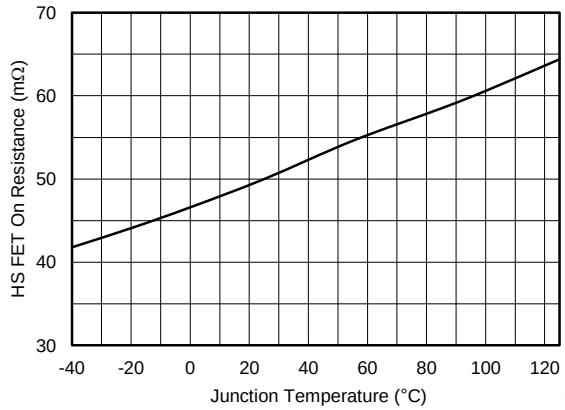


Figure 1. High-Side MOSFET On Resistance vs Junction Temperature

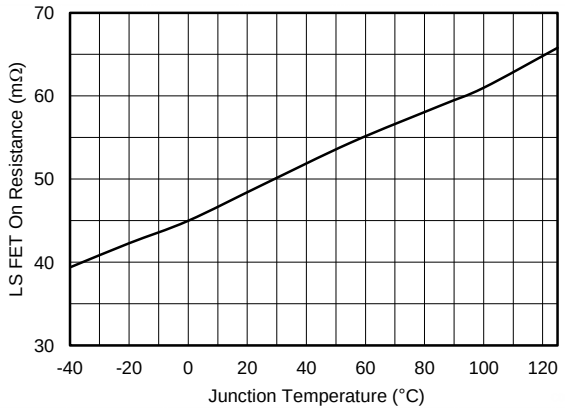


Figure 2. Low-Side MOSFET On Resistance vs Junction Temperature

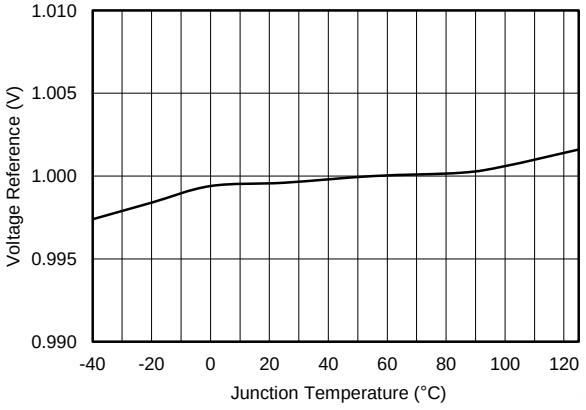


Figure 3. Voltage Reference vs Junction Temperature

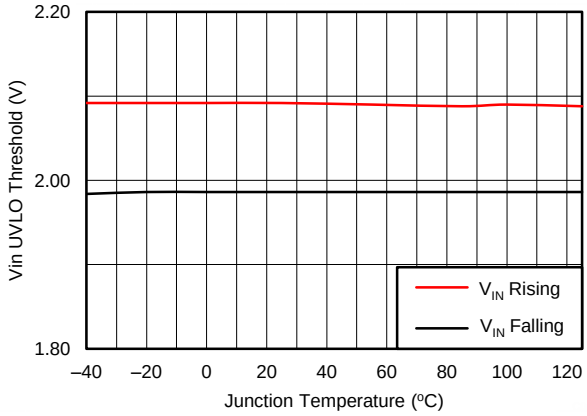


Figure 4. Vin UVLO Threshold vs Junction Temperature

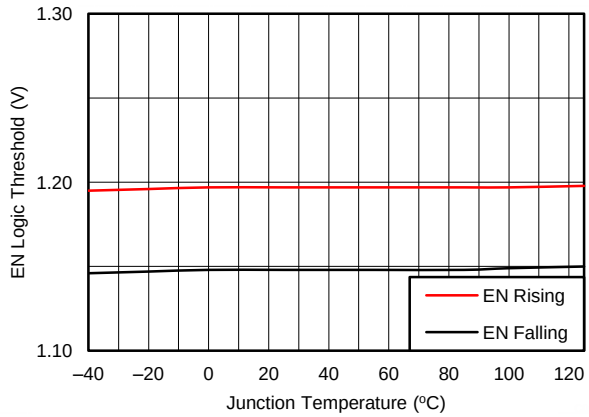


Figure 5. EN Logic Threshold vs Junction Temperature

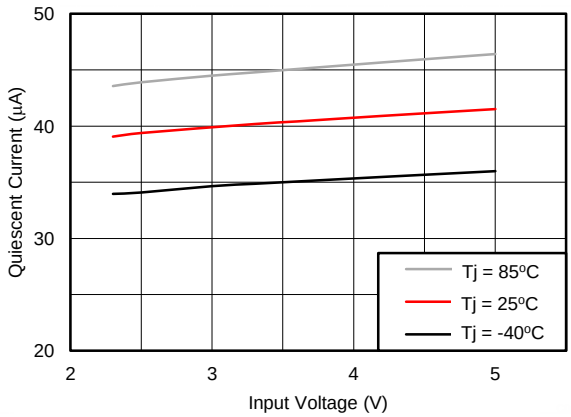


Figure 6. Quiescent Current vs Input Voltage (Boost Mode)

Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = -40°C to 125 °C, unless otherwise noted.

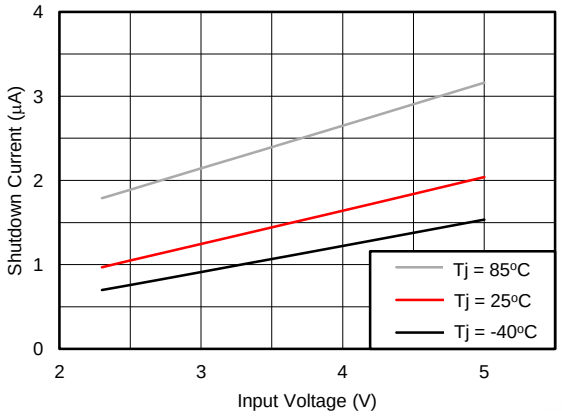


Figure 7. Shutdown Current vs Input Voltage (Boost Mode)

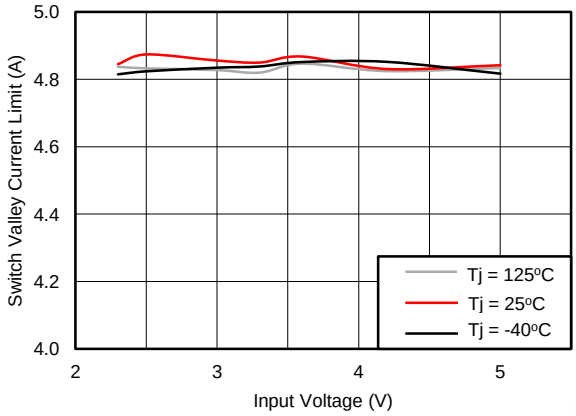


Figure 8. Switch Valley Current Limit vs Input Voltage (Boost Mode)

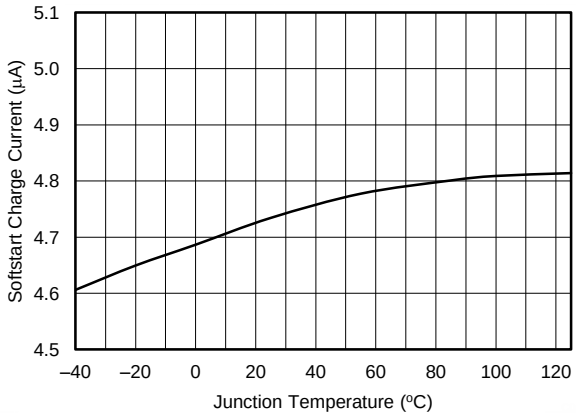


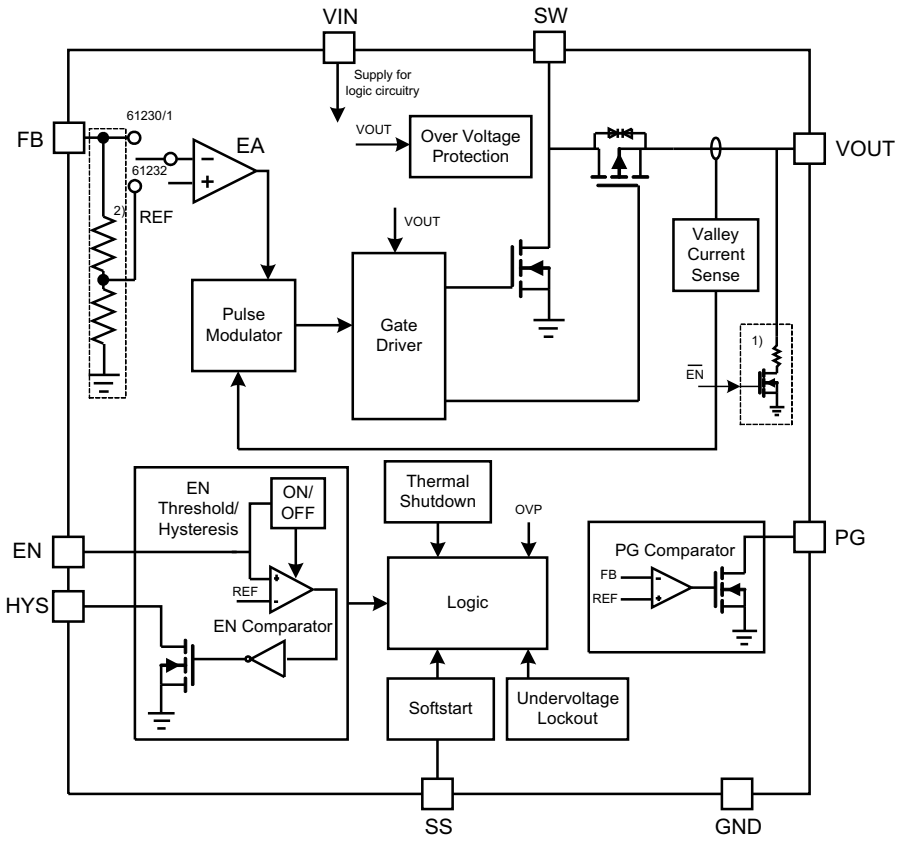
Figure 9. Soft Start Charge Current vs Junction Temperature

8 Detailed Description

8.1 Overview

The TPS6123x synchronous step-up converter typically operates at a quasi-constant 2-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6123x converter operates in power-save mode with pulse frequency modulation (PFM). The converter uses a novel quasi-constant on-time valley current mode control scheme which provides excellent transient line / load response with minimal output capacitance. Internal loop compensation simplifies the design process while minimizing the number of external components. The TPS6123x device can smoothly transit in and out of zero duty cycle mode (high side FET full on). Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive.

8.2 Functional Block Diagram



(1) Output discharge block is implemented in TPS61231 only.

(2) Internal resistor divider is implemented in TPS61232 only. For adjustable output versions, the FB pin is directly connected to the negative pin of the EA.

8.3 Feature Description

8.3.1 Startup

In boost mode (PWM or PFM), the rectifying switch is turned on first until the output capacitor is charged to 0.5 V with the current limit of 550 mA after the device is enabled. Then, the output capacitor is continuously charged to a value close to the input voltage. This is called the pre-charge phase. During the pre-charge phase, the output current is limited by the pre-charge current limit of the high side rectifying switch and the SS pin voltage follows the FB voltage (in the TPS61232, the SS pin follows the internal FB voltage). Once the output capacitor has been biased to the input voltage, the device starts switching. This is called the soft start phase. During the soft

Feature Description (continued)

start phase, the SS pin voltage limits the FB pin voltage, and the output voltage rising slope follows the SS pin voltage slope. The capacitor connected to the SS pin is charged by the internal bias current of I_{SS}, giving the time of the soft start phase shown in Equation 1. The larger the soft start capacitor, the longer the soft start phase time. Leaving the SS pin floating sets the minimum soft startup phase time. The device finishes the soft start phase and operates normally when the nominal output voltage is reached.

$$t_{SS} = \frac{C_{SS}}{5\,\mu A} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times V_{REF} \quad (1)$$

The SS pin voltage is discharged in the cases when the device gets disabled by the EN pin, thermal shutdown and undervoltage lockout. The SS pin may be left floating to disable the soft start phase and start up with the fastest time. In zero duty cycle mode, only the pre-charge phase works during startup.

8.3.2 Current Limit Operation

The device employs a valley current sensing scheme. Switch valley current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier. If the current is above the valley current limit level when it is time to turn off the synchronous rectifier, the device instead keeps the synchronous rectifier on until its current decreases below the valley current limit level. The maximum continuous output current $I_{OUT(MAX)}$, before entering switch valley current limit operation, is defined by Equation 2.

$$I_{OUT(MAX)} = (1-D) \times \left(I_{LIM\_SW} + \frac{1}{2}\Delta I_L\right)$$

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_{SW}} \quad (2)$$

Where

I_{LIM_SW} = Switch valley current limit
L = Inductor value
f_{SW} = Switching frequency

When the switch current limit is reached, the output voltage decreases from further load increase. The switch valley current limit works in PWM, PFM and Zero Duty Cycle Mode operations.

Another current limit scheme, pre-charge current limit, I_{LIM_Pre} is implemented. Pre-charge current limit detection works when $V_{OUT} < V_{OUT\_NOM}$ and $V_{OUT} < V_{IN}$. It can happen when the device is in the pre-charge phase or an over load condition. It impacts the minimum load resistance at startup as shown in Figure 14 and Figure 27.

8.3.3 Enable/Disable

The EN pin is connected to an ON/OFF detector (ON/OFF) and an input of the Enable Comparator, shown in the functional block diagram. With a voltage level of 0.4 V or less at the EN pin, the ON/OFF detector turns the device into Shutdown mode and the quiescent current is reduced to typically 1.5 uA. In this mode, the EN comparator and the entire internal control circuitry are switched off. A voltage level of typically 0.9 V at the EN pin triggers the ON/OFF detector and activates the internal reference, the EN comparator and the UVLO comparator. Once the ON/OFF detector has tripped, the quiescent current into the VIN pin is typically 1.5 µA.

The TPS6123x starts regulation once the voltage at the EN pin trips the threshold $V_{EN\_TH\_ON}$ and the VIN pin voltage is above the UVLO threshold. The device enters startup and ramps up the output voltage. The TPS6123x stops regulation once the voltage on the EN pin falls blow the threshold $V_{EN\_TH\_OFF}$ or the VIN pin voltage falls below the UVLO threshold. For proper operation, The EN pin must be terminated and must not be left floating. An external logic signal applied directly to the EN pin can enable/disable the device. The device can be driven into shutdown mode by pulling the EN pin to GND. In this mode, true load disconnect between the battery and load prevents current flow from V_{IN} to V_{OUT}, as well as reverse flow from V_{OUT} to V_{IN}.

Feature Description (continued)

8.3.4 Undervoltage Lockout

An under voltage lockout is implemented to avoid mis-operation of the device at low input voltages. It shuts down the device with voltages lower than V_{UVLO}.

Use the HYS pin to configure a new undervoltage lockout threshold and hysteresis shown in Figure 10 and Equation 3. The new thresholds must be higher than V_{UVLO}; otherwise it does not work. The devices holds the HYS pin low until the EN voltage rises above $V_{EN\_TH\_ON}$. Then, the HYS pin goes high impedance.

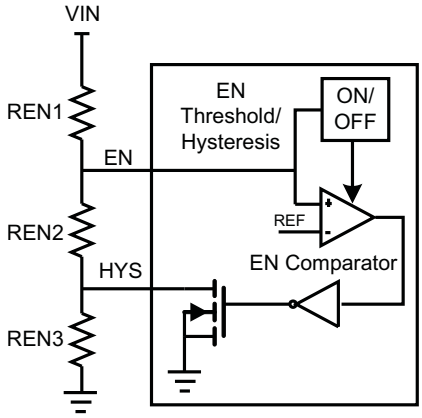


Figure 10. EN Comparator threshold and hysteresis setting

$$V_{IN\_OFF} = V_{TH\_EN\_OFF} \times \left(1 + \frac{REN1}{REN2 + REN3}\right) = 1.14V \times \left(1 + \frac{REN1}{REN2 + REN3}\right)$$
$$V_{IN\_ON} = V_{TH\_EN\_ON} \times \left(1 + \frac{REN1}{REN2}\right) = 1.19V \times \left(1 + \frac{REN1}{REN2}\right) \quad (3)$$

8.3.5 Output Capacitor Discharge, TPS61231

To make sure the device starts up under defined conditions, the output capacitor of the TPS61231 gets discharged by the VOUT pin with a typical discharge resistor of R_{DIS} in the cases when the device gets disabled by the EN pin, thermal shutdown, and undervoltage lockout.

8.3.6 Power Good Output

The PG output is low when the output voltage is below 90% of its nominal value. The PG pin becomes high impedance once the output is higher than 95% of its nominal voltage. The PG pin is an open drain output and is specified to sink up to 500 µA. This PG output requires a pull-up resistor that cannot be connected to any voltage higher than 5.5 V. PG is held low when the device is disabled by the EN pin and thermal shutdown.

8.3.7 Over Voltage Protection

The device stops switching as soon as the output voltage exceeds V_{OVP}. When the output voltage falls 0.15V below the OVP threshold, the device resumes normal operation until the output voltage exceeds the OVP threshold again.

8.3.8 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the junction temperature falls below the threshold, it returns to normal operation automatically.

8.4 Device Functional Modes

The TPS6123x boost converter family has three operation modes, as shown in Table 1.

Table 1. Operation Mode Description

MODE	DESCRIPTION	CONDITION
PWM	Boost in normal switching operation	$V_{IN} < V_{OUT}$ + 0.2 V, heavy load
PFM	Boost in power save operation	$V_{IN} < V_{OUT}$ + 0.2 V, light load
Zero Duty Cycle	Zero duty cycle operation	$V_{OUT} < V_{IN} \le V_{OUT}$ + 0.24 V and $V_{OUT} \ge V_{OUT\_NOM}$

8.4.1 Boost Normal Mode

The TPS6123x boost converter family typically operates at a quasi-constant 2-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch, shown in the functional block diagram, is turned on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once this peak current is reached, the current comparator trips, the on-timer is reset turning off the low-side N-MOS switch and turning on the high-side rectifying switch. The current through the inductor then decays to an internally set valley current. Once this occurs, the on-timer is set to turn the boost switch back on again and the cycle is repeated.

8.4.2 Boost Power Save Mode

The device integrates a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. In power save mode, the device only switches when the output voltage trips below a set threshold voltage. It ramps up the output with several pulses and enters the power save mode when the output voltage exceeds the set threshold voltage. PFM is left and PWM mode entered when the inductor current becomes discontinuous. The DC output voltage in PFM mode rises above the nominal output voltage in PWM mode by 0.7%.

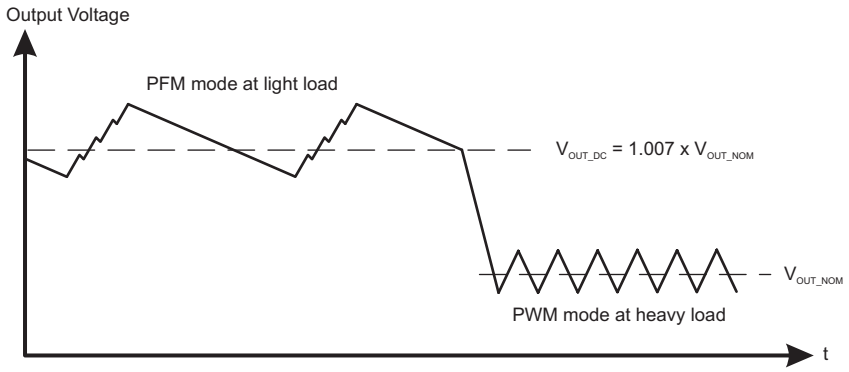


Figure 11. Output Voltage in PFM/PWM Mode

8.4.3 Zero Duty Cycle Mode

When the input voltage is lower than V_{OUT} + 0.24 V and V_{OUT} is higher than the nominal output voltage, the device automatically changes to a Zero Duty Cycle Mode. In Zero Duty Cycle Mode, the rectifying switch is constantly turned on and the low side switch is turned off. The output voltage in this mode depends on the resistance between the input and the output, calculated as:

$$V_{OUT} = V_{IN} - I_{OUT} \times (R_{DS(on)} + R_L) \quad (4)$$

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are designed to operate from an input voltage supply range between 2.3 V and 5.5 V with a maximum output current of 2.1 A. The devices operate in PWM mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode the TPS6123x converter operates with the nominal switching frequency of 2 MHz which provides a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. See the *Related Documentation* section for additional documentation.

9.2 Typical Applications

9.2.1 TPS61230 2.3-V to 5.5-V Input, 5-V Output Converter

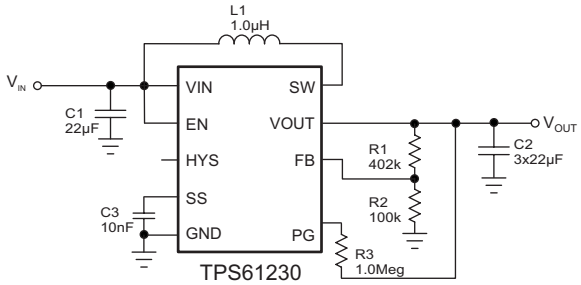


Figure 12. TPS61230 5-V Output Typical Application

9.2.1.1 TPS61230 5-V Output Design Requirements

Use the following typical application design procedure to select external components values for the TPS61230 device.

Table 2. TPS61230 5-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.3 V to 5.5 V
Output Voltage	5.0 V
Output Voltage Ripple	±3% V_{OUT}
Transient Response	±10% V_{OUT}
Input Voltage Ripple	±200 mV
Output Current Rating	2.1 A
Operating Frequency	2 MHz

9.2.1.2 TPS61230 5-V Detailed Design Procedure

Table 3. TPS61230 5-V Output List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
L1	1.0 µH, power inductor, XFL4020-102MEB	Coilcraft
C1	2 µF 6.3 V, 0805, X5R ceramic, GRM21BR60J226ME39	Murata
C2	3 × 22 µF 10 V, 0805, X5R ceramic, LMK212BBJ226MG	YUDEN
C3	10 nF, X7R ceramic	Murata
R1	402 k, resistor, chip, 1/10W, 1%	Rohm
R2	100 k, resistor, chip, 1/10W, 1%	Rohm

9.2.1.2.1 Programming the Output Voltage

The TPS6123x device family's output voltage need to be programmed via an external voltage divider to set the desired output voltage.

An external resistor divider is used, as shown in Equation 5. By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{FB}. The following equation can be used to calculate R1 and R2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 1V \times \left(1 + \frac{R1}{R2}\right) \quad (5)$$

For best accuracy, R2 should be kept smaller than 100 kΩ to ensure that the current following through R2 is at least 100 times larger than FB pin leakage current. Changing R2 towards a lower value increases the robustness against noise injection. Changing the R2 towards higher values reduces the quiescent current for achieving highest efficiency at low load currents.

For the fixed output voltage version, TPS61232, the FB pin must be tied to the output directly.

9.2.1.2.2 Inductor and Capacitor Selection

The second step is the selection of the inductor and capacitor components. To simplify this process, Table 4 outlines possible inductor and output capacitor value combinations.

Table 4. Inductor and Output Capacitor Combinations

L (µH)(1)	C_{OUT} (µF)(2)			
	10	20	47	100
0.47		√	√	√
1.0		√(3)	√	√
1.5				

(1) This is the nominal inductance of inductor. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by -30%.
(2) This is the effective capacitance of output capacitors. A higher nominal value is required.
(3) Typical application configuration. Other check mark indicates alternative filter combinations.

9.2.1.2.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches. The inductor peak current varies as a function of the load, the input and output voltages and is estimated using Equation 6.

$$I_{L(PEAK)} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \quad (6)$$

Where

η = Power conversion estimated efficiency

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce reliability. It's recommended to choose the saturation current for the inductor 20%~30% higher than the $I_{L(PEAK)}$, from Equation 6. The following inductors are recommended to be used in designs.

Table 5. List of Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DC RESISTANCE [mΩ]	PART NUMBER	MANUFACTURER
1.0	5.4	10.8	XFL4020-102ME	Coilcraft
1.0	7.5	9	LQH6PPN1R0	muRata
0.47	6.6	7.6	XFL4015-471ME	Coilcraft

9.2.1.2.2.2 Output Capacitor Selection

For the output capacitor, it is recommended to use small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic capacitor of 1 µF in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

Care must be taken when evaluating a capacitor's derating under bias. The bias can significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

The ESR impact on the output ripple must be considered as well, if tantalum or electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{Ripple} is:

$$V_{Ripple(ESR)} = I_{L(PEAK)} \times ESR \tag{7}$$

9.2.1.2.2.3 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source to reduce ringing than can occur between the inductance of the power source leads and C_{IN}.

9.2.1.2.3 Loop Stability, Feed Forward Capacitor

The third step is to check the loop stability. The stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple, $V_{Ripple(OUT)}$

When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

The load transient response is another approach to check the loop stability. During the load transient recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

As for the heavy load transient applications such as a 2 A load step transient, a feed forward capacitor in parallel with R1 is recommended. The feed forward capacitor increases the loop bandwidth by adding a zero. This results in a lower output voltage drop, as shown in Figure 36. Set the feed forward capacitor zero near 20 kHz for most applications. See application report *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289).

9.2.1.3 TPS61230 5-V Output Application Performance Plots

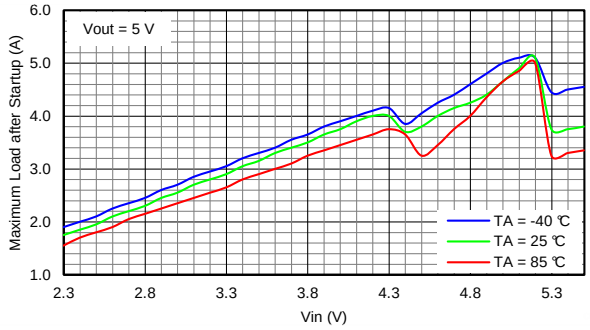


Figure 13. Maximum Load Current after Startup

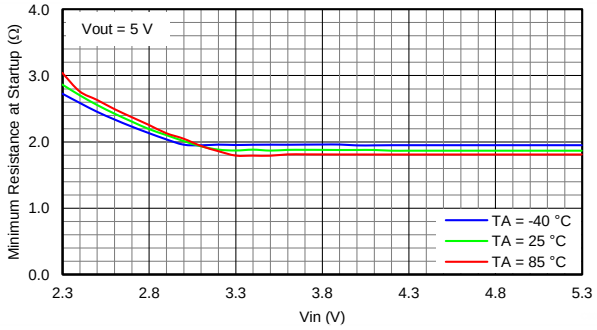


Figure 14. Minimum Resistance at Startup

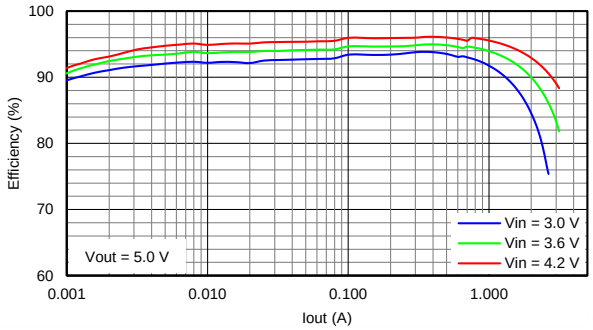


Figure 15. Efficiency

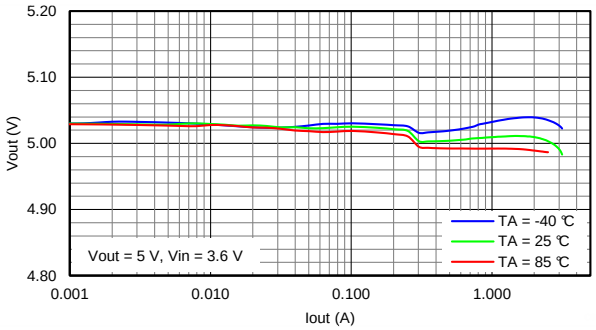


Figure 16. Load Regulation

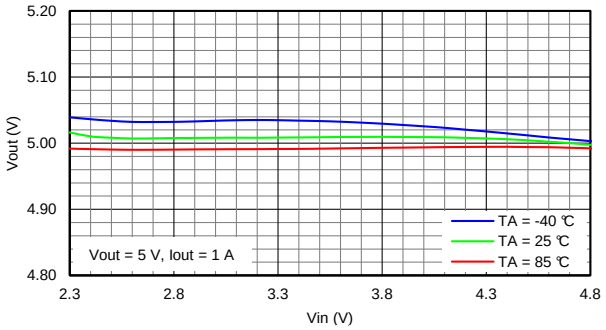


Figure 17. Line Regulation

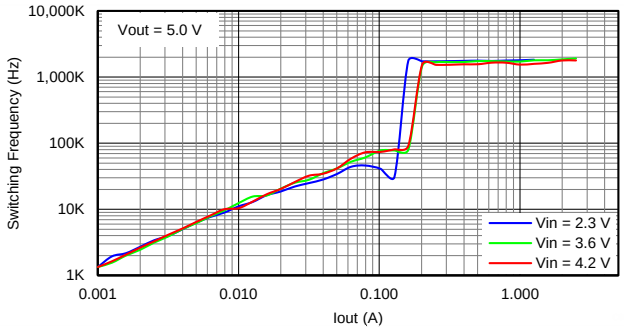


Figure 18. Switching Frequency

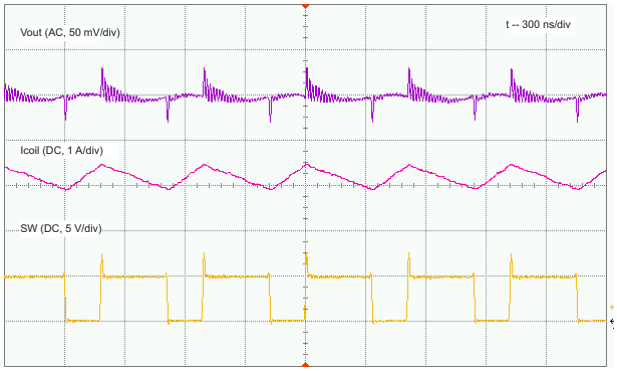


Figure 19. PWM Operation (V_{OUT} = 5 V, I_{OUT} = 2 A)

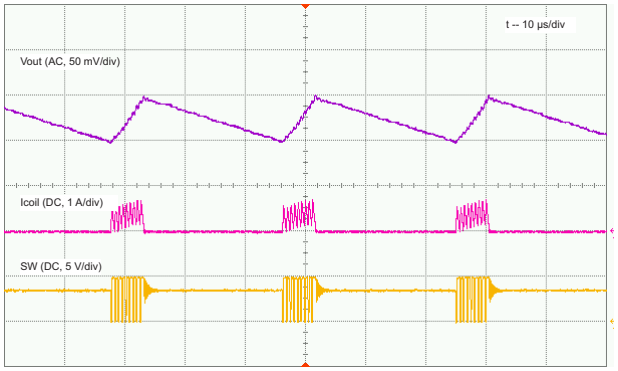


Figure 20. PFM Operation (V_{OUT} = 5 V, I_{OUT} = 50 mA)

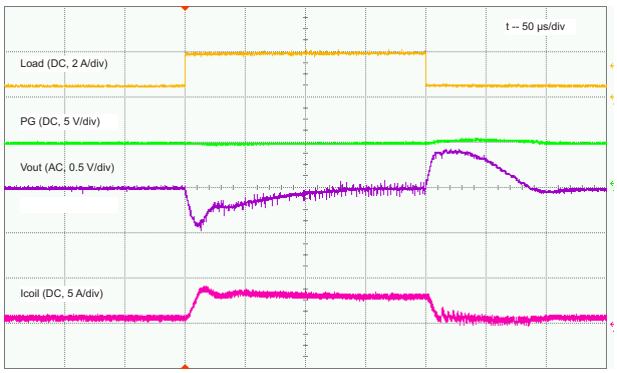


Figure 21. Load Transient (V_{OUT} = 5 V, I_{OUT} = 0.5 A to 2 A)

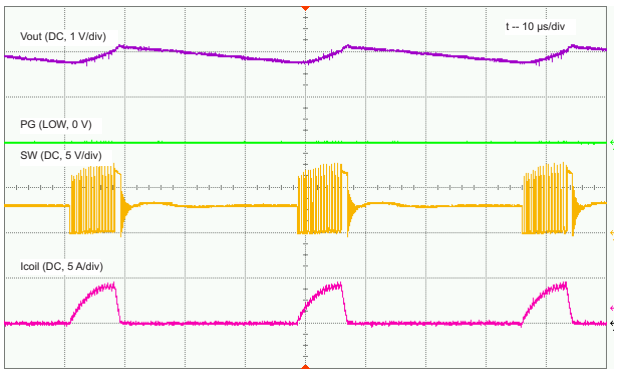


Figure 22. Output Over Voltage Protection (FB = 0 V, R_{OUT} = 30 Ω)

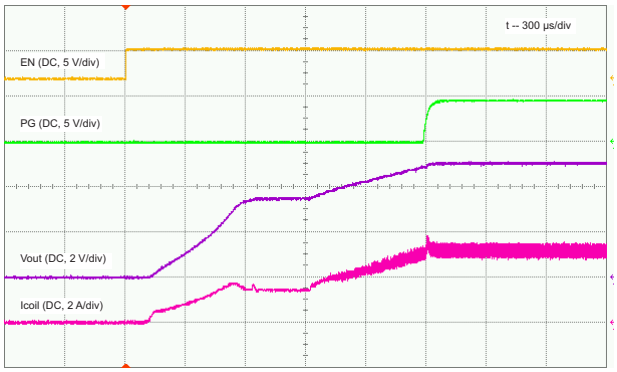


Figure 23. Startup (V_{OUT} = 5 V, R_{OUT} = 2.5 Ω)

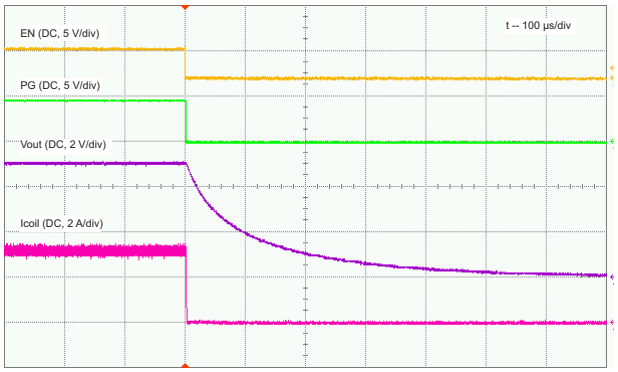


Figure 24. Shutdown (V_{OUT} = 5 V, R_{OUT} = 2.5 Ω)

9.2.2 TPS61230 2.3-V to 5.5-V Input, 3.5-V Output Converter

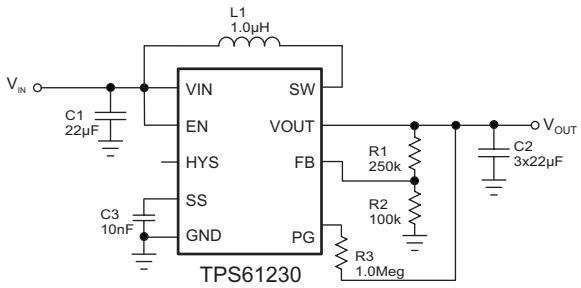


Figure 25. TPS61230 3.5-V Output Typical Application

9.2.2.1 TPS61230 3.5-V Output Design Requirements

Table 6. TPS61230 3.5-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.3 V to 5.5 V
Output Voltage	3.5 V
Output Voltage Ripple	±3% V_{OUT}
Transient Response	±10% V_{OUT}
Input Voltage Ripple	±200 mV
Output Current Rating	2.1 A
Operating Frequency	2 MHz

9.2.2.2 Detailed Design Procedure

Refer to the *TPS61230 5-V Detailed Design Procedure* section for the 3.5-V detailed design procedures.

9.2.2.3 TPS61230 3.5-V Output Application Performance Plots

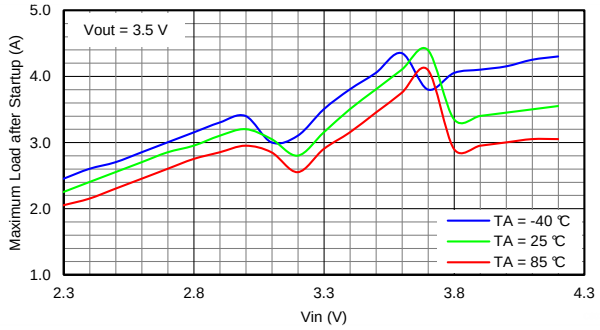


Figure 26. Maximum Load Current after Startup

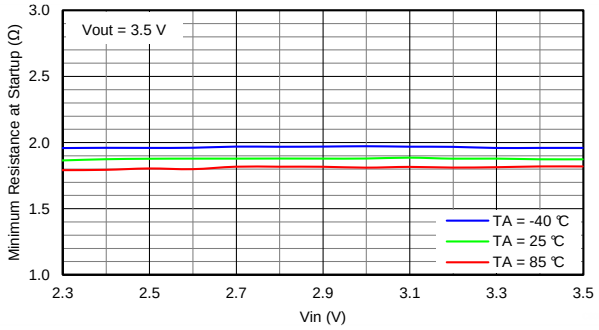


Figure 27. Minimum Resistance at Startup

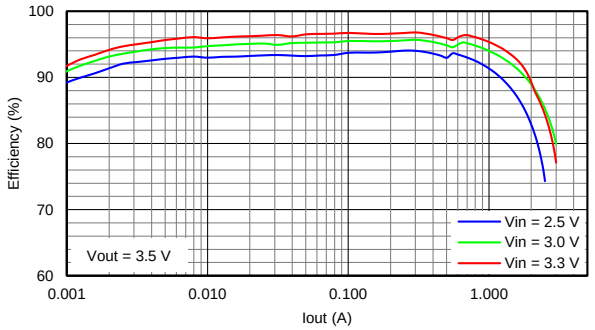


Figure 28. Efficiency

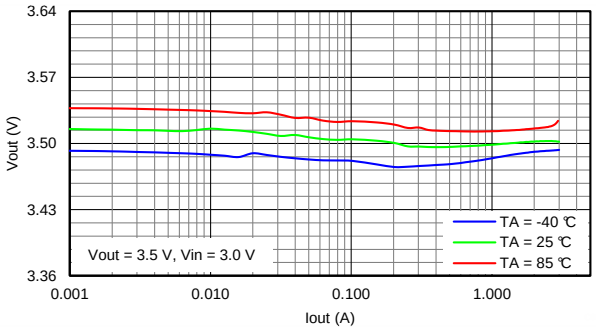


Figure 29. Load Regulation

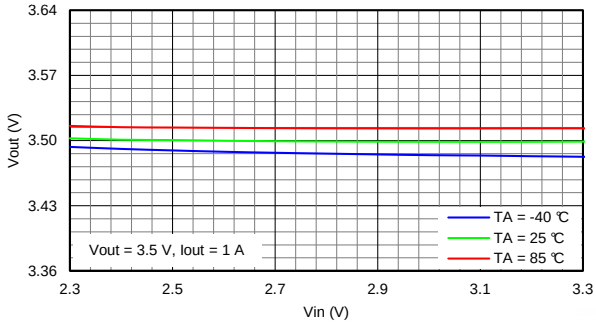


Figure 30. Line Regulation

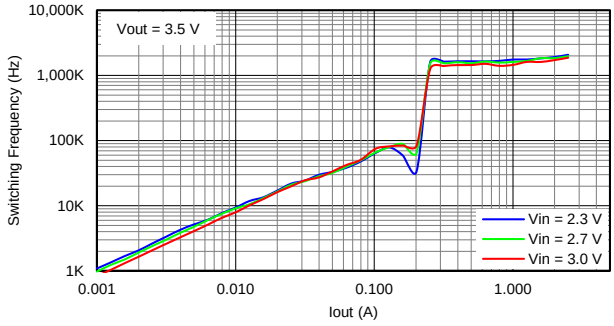


Figure 31. Switching Frequency

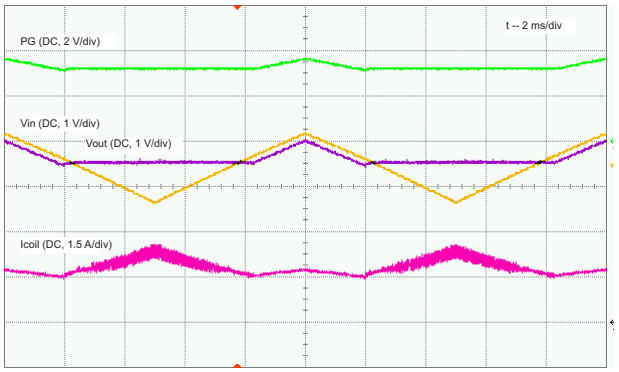


Figure 32. Input Sweep (V_{OUT} = 3.5 V, V_{IN} = 2.7 V to 4.2 V, I_{OUT} = 1.5 A)

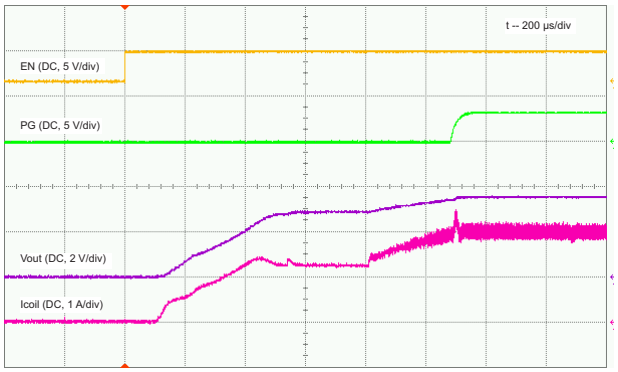


Figure 33. Startup (V_{OUT} = 3.5 V, V_{IN} = 3.0 V, R_{OUT} = 2.3 Ω)

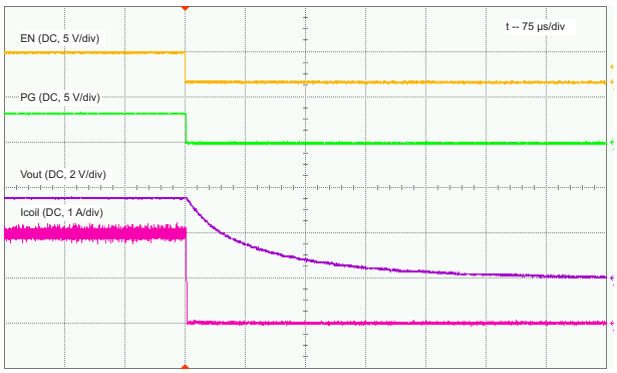


Figure 34. Shutdown (V_{OUT} = 3.5 V, V_{IN} = 3.0 V, R_{OUT} = 2.3 Ω)

9.2.3 TPS61230 Application with Feed Forward Capacitor for Best Transient Response

As for the heavy load transient applications such as a 2-A load step transient, a feed forward capacitor in parallel with R1 is recommended. The feed forward capacitor increases the loop bandwidth by adding a zero. This results in a lower output voltage drop, as shown in Figure 36. Set the feed forward capacitor zero near 20 kHz for most applications. See application report *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289).

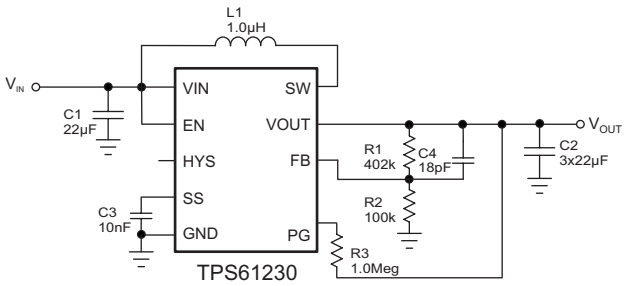


Figure 35. TPS61230 5-V Output with Cff Typical Application

9.2.3.1 Design Requirements

Refer to the *TPS61230 5-V Output Design Requirements* section for the design requirements.

9.2.3.2 Detailed Design Procedure

Refer to the *TPS61230 5-V Detailed Design Procedure* section for the detailed design procedures.

9.2.3.3 Application Curve

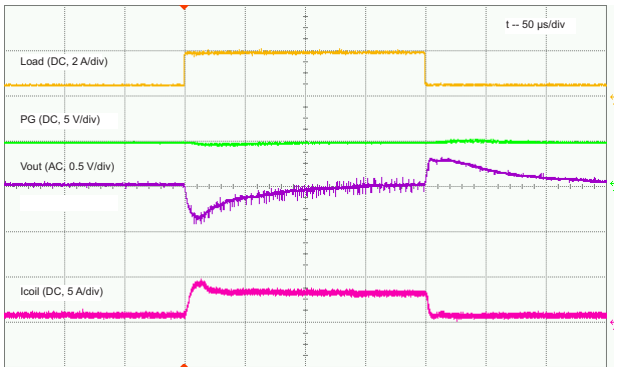


Figure 36. Load Transient (V_{OUT} = 5 V, I_{OUT} = 0.5 A to 2 A, C_{FF} = 18 pF)

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.3 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at the GND pin of the IC. The most critical current path for all boost converters is from the switching FET, through the synchronous FET, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the IC's VOUT and GND pin.

See Figure 37 for the recommended layout.

11.2 Layout Example

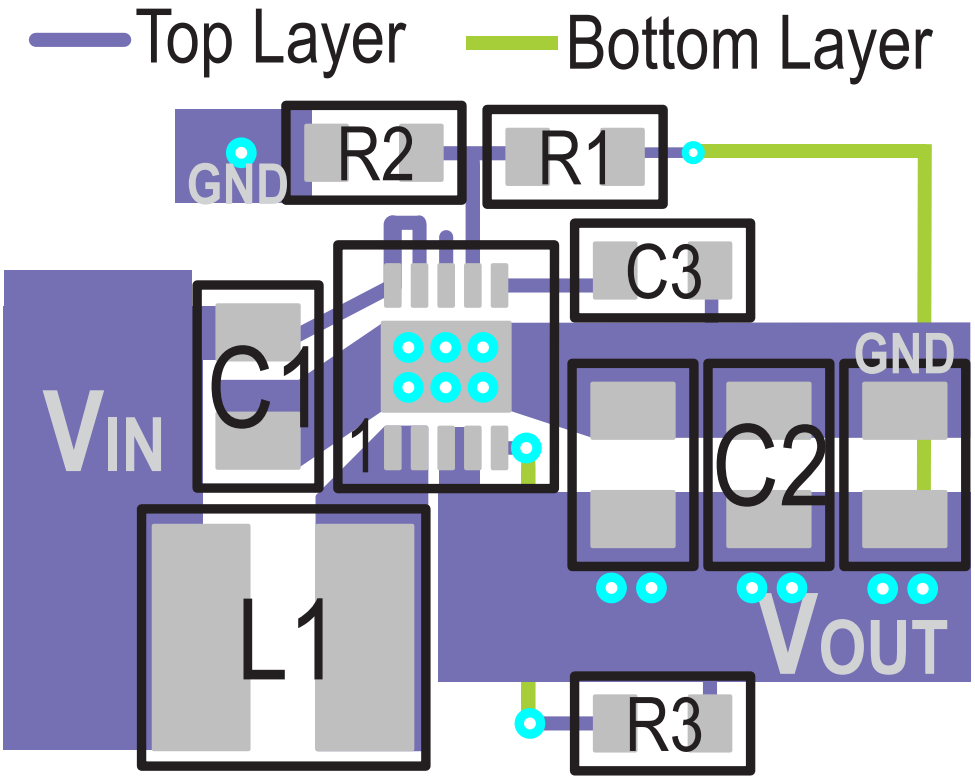


Figure 37. Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

Thermal Considerations (continued)

For more details on how to use the thermal parameters in the dissipation ratings table please check the application report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017) and the application report *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor SLVA289

Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs (SZZA017)

Semiconductor and IC Package Thermal Metrics (SPRA953)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61230	Click here	Click here	Click here	Click here	Click here
TPS61231	Click here	Click here	Click here	Click here	Click here
TPS61232	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61230DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBK	Samples
TPS61230DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBK	Samples
TPS61232DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBL	Samples
TPS61232DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

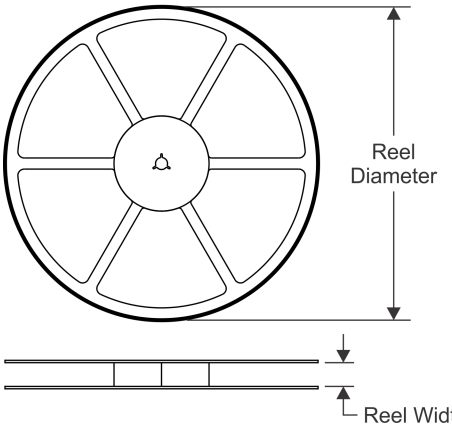
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

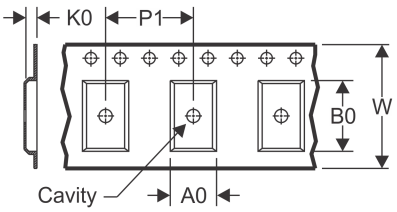
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

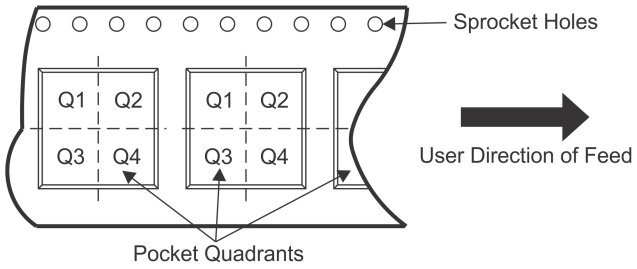


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

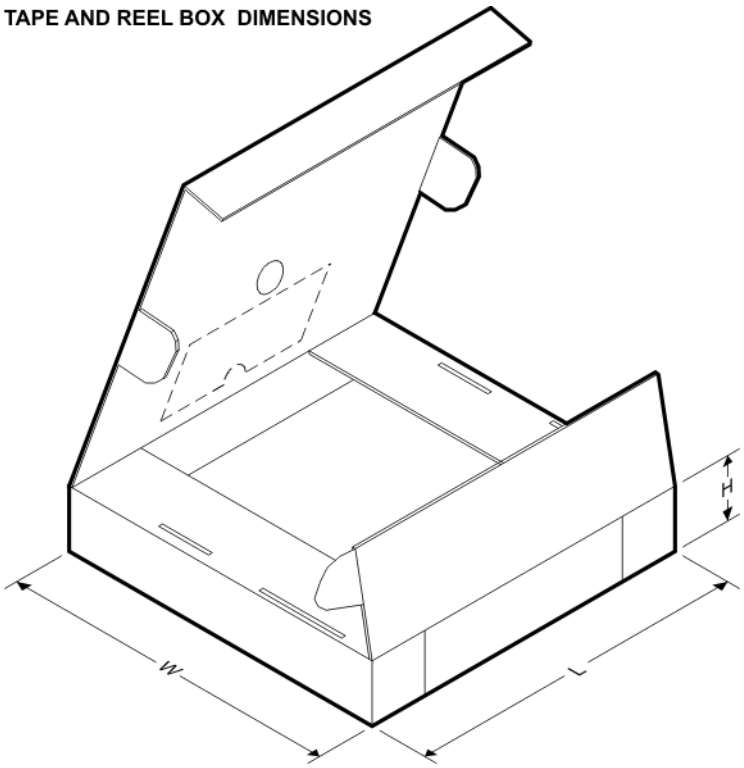
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61230DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61230DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61232DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61232DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

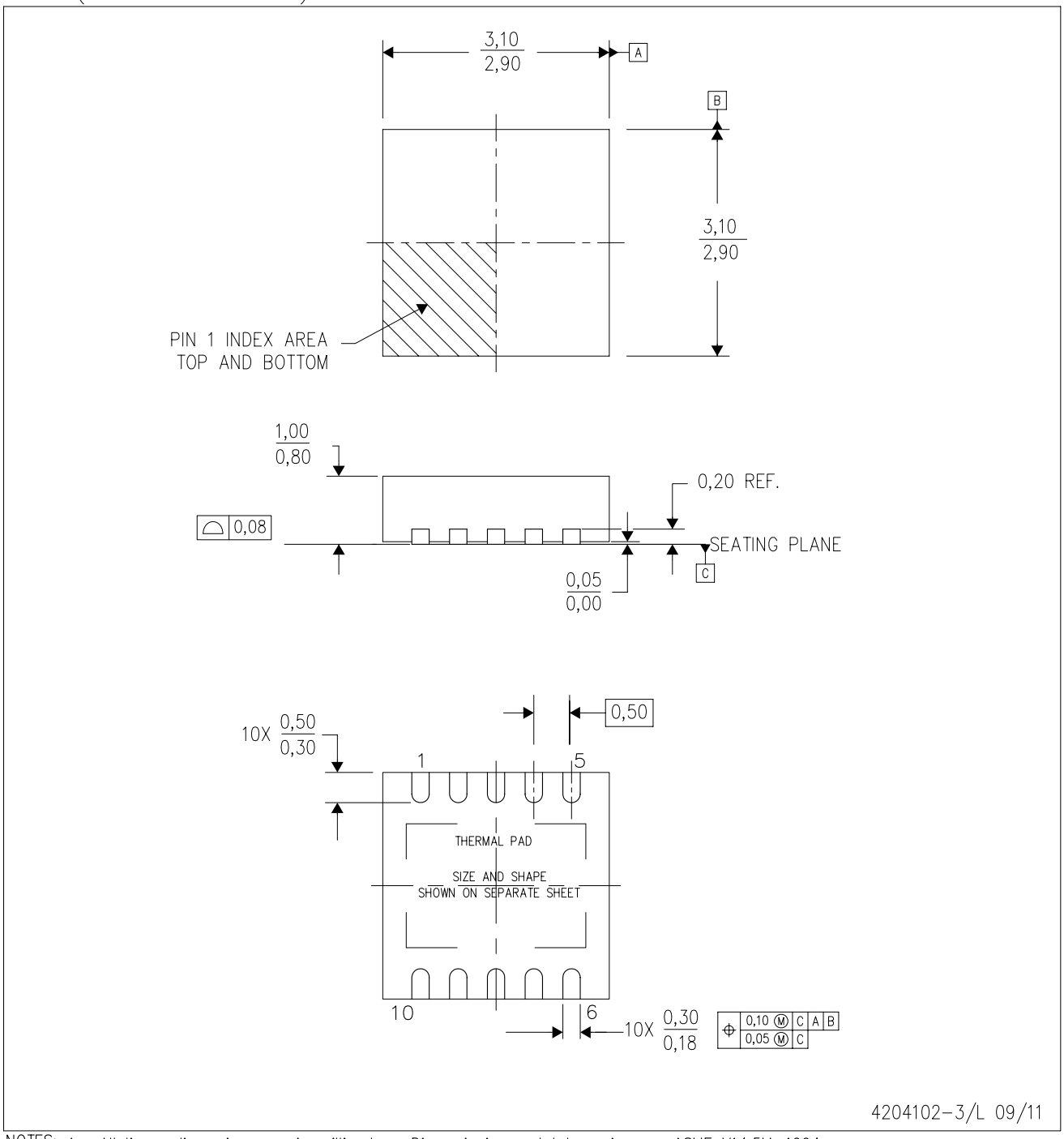
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61230DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61230DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61232DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61232DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

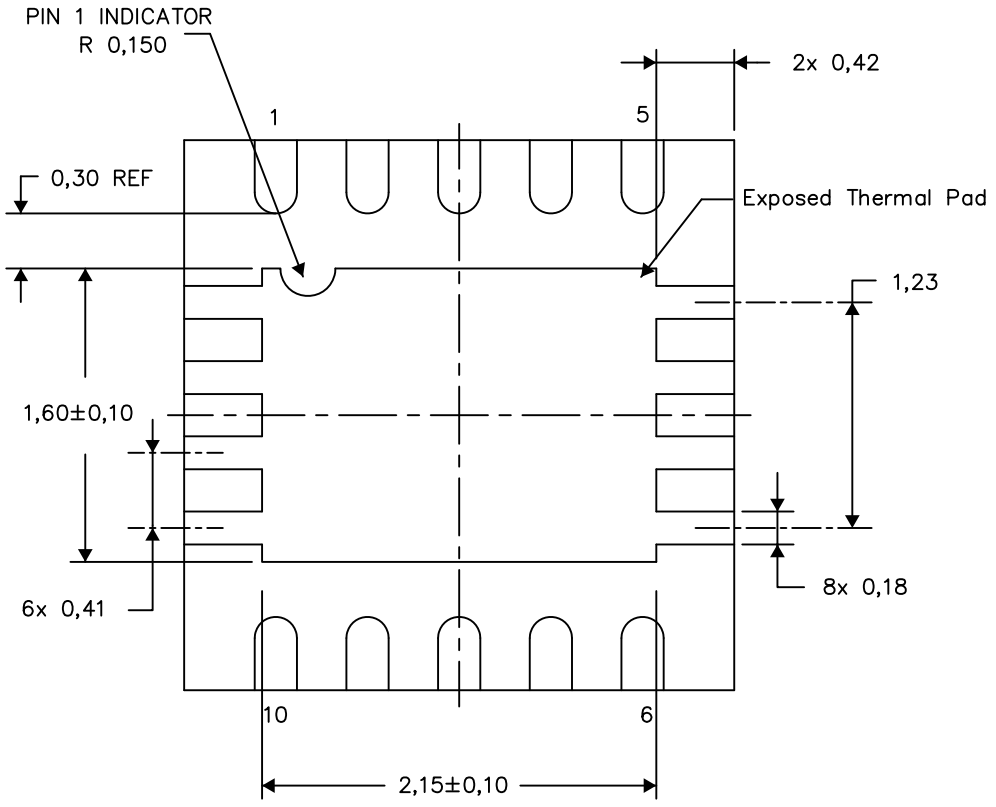
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



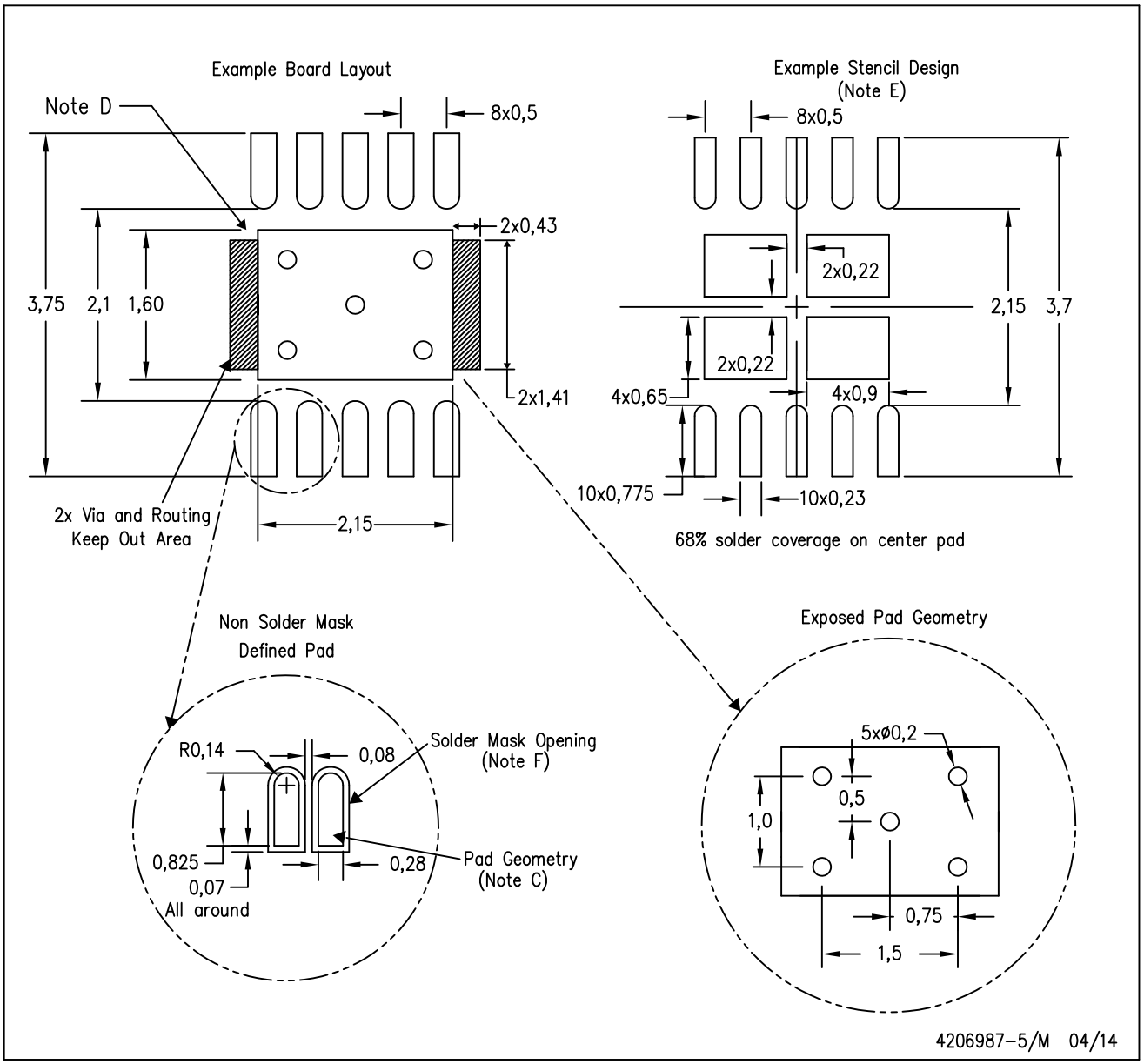
Bottom View

Exposed Thermal Pad Dimensions

4206565–9/U 04/14

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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